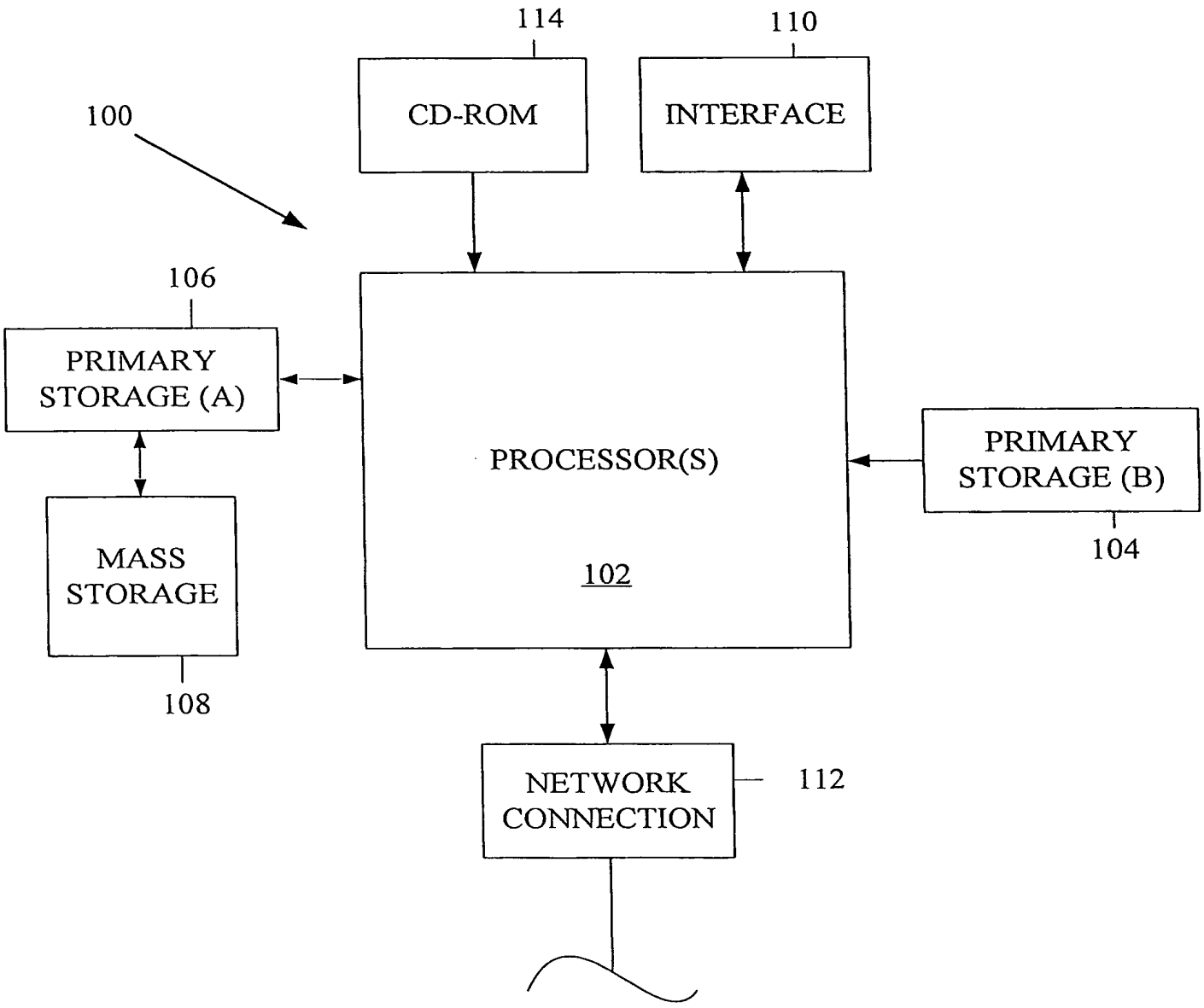

114
110
CD-ROM
INTERFACE
100
106
PRIMARY STORAGE (A)
PROCESSOR(S)
102
PRIMARY STORAGE (B)
104
MASS STORAGE
108
NETWORK CONNECTION
112

Figure 1

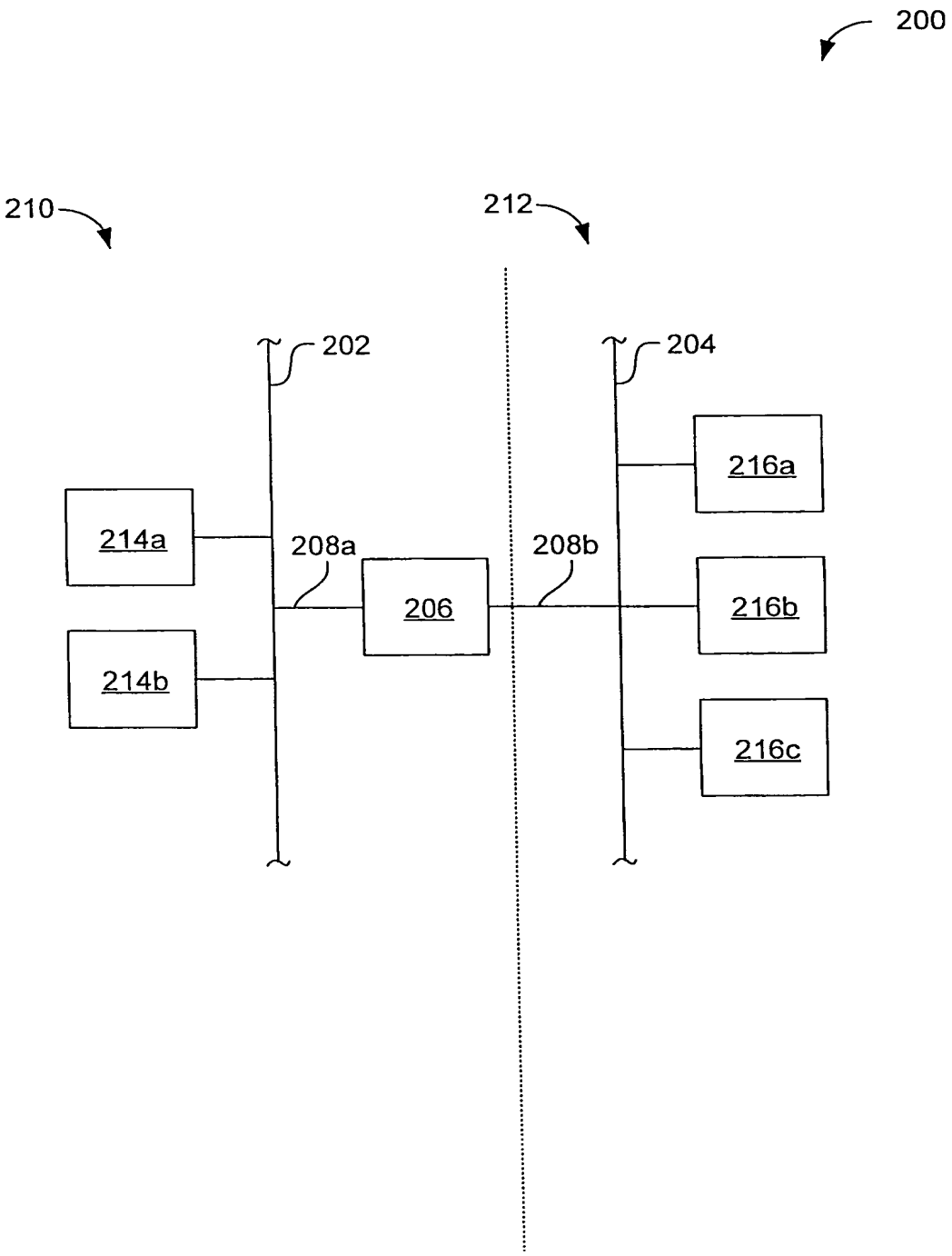


Figure 2

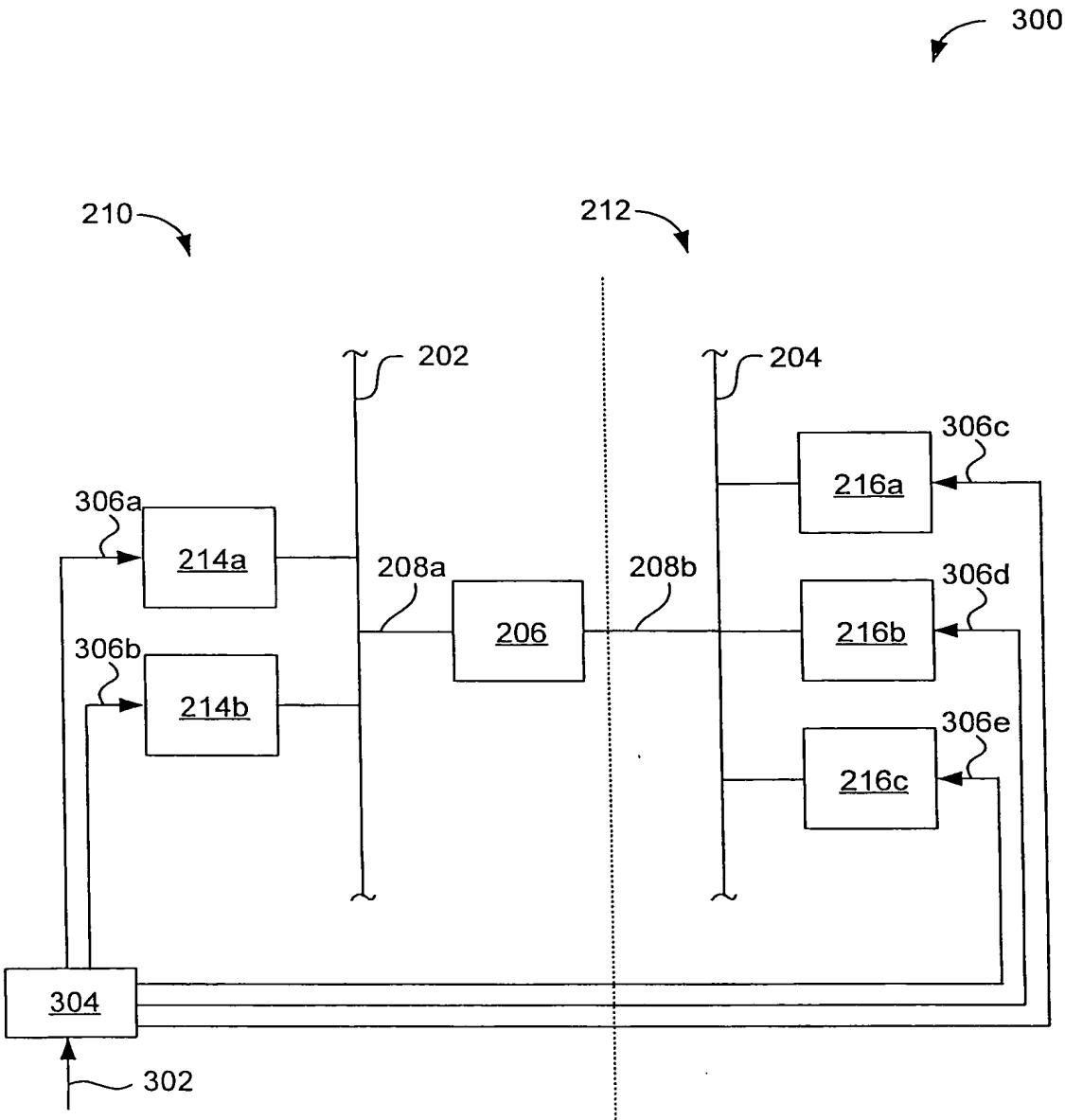
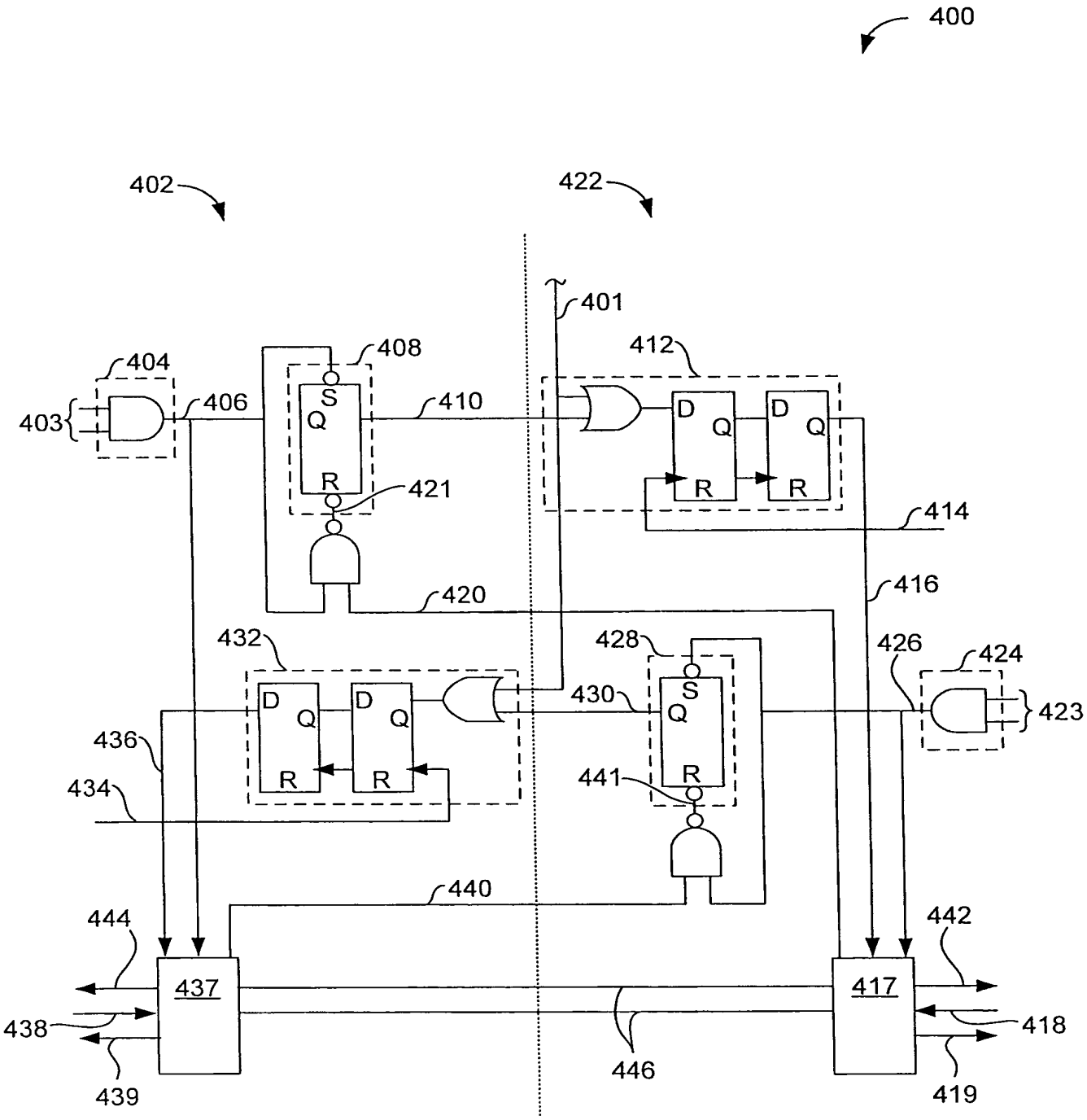

300
210
212
202
204
306a
214a
208a
206
208b
306c
216a
306d
216b
306b
214b
306e
216c
304
302

Figure 3


400
402
422
401
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412
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410
S
Q
R
D
Q
R
421
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Figure 4

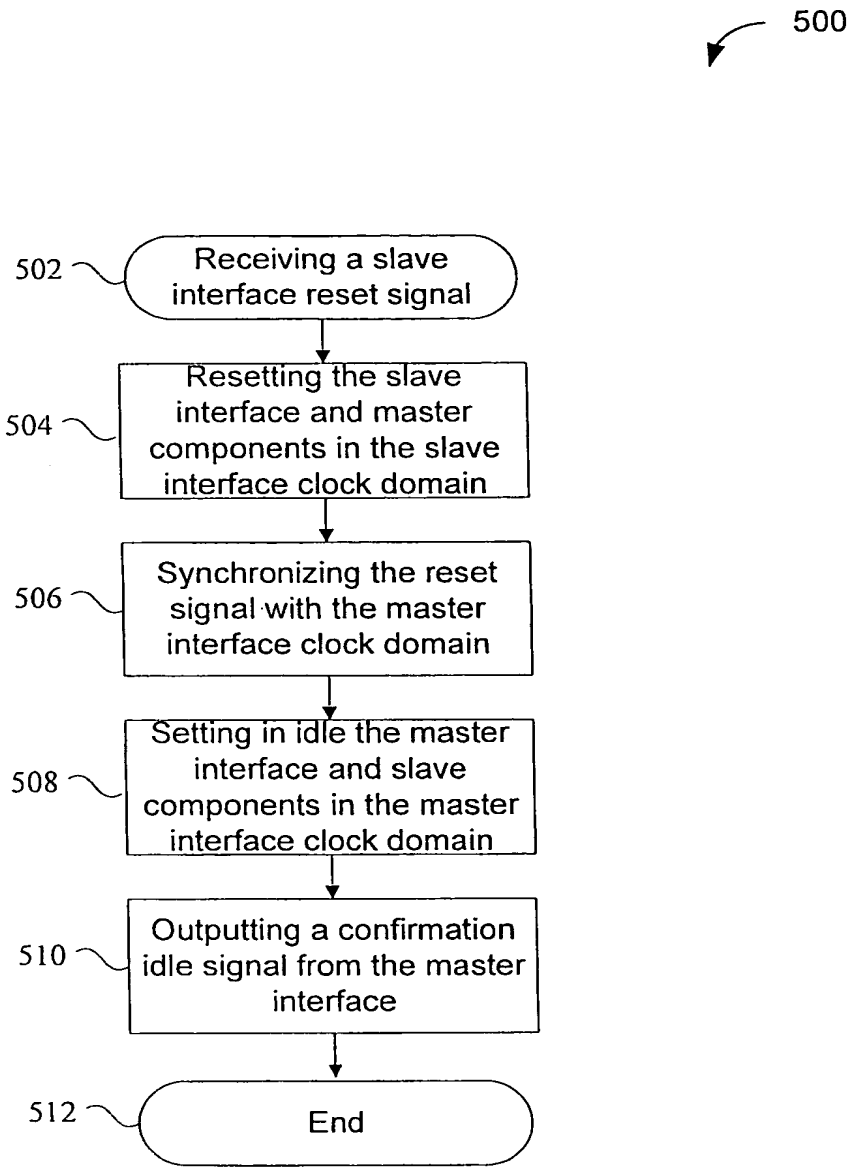
500
502
Receiving a slave interface reset signal
504
Resetting the slave interface and master components in the slave interface clock domain
506
Synchronizing the reset signal with the master interface clock domain
508
Setting in idle the master interface and slave components in the master interface clock domain
510
Outputting a confirmation idle signal from the master interface
512
End

Figure 5

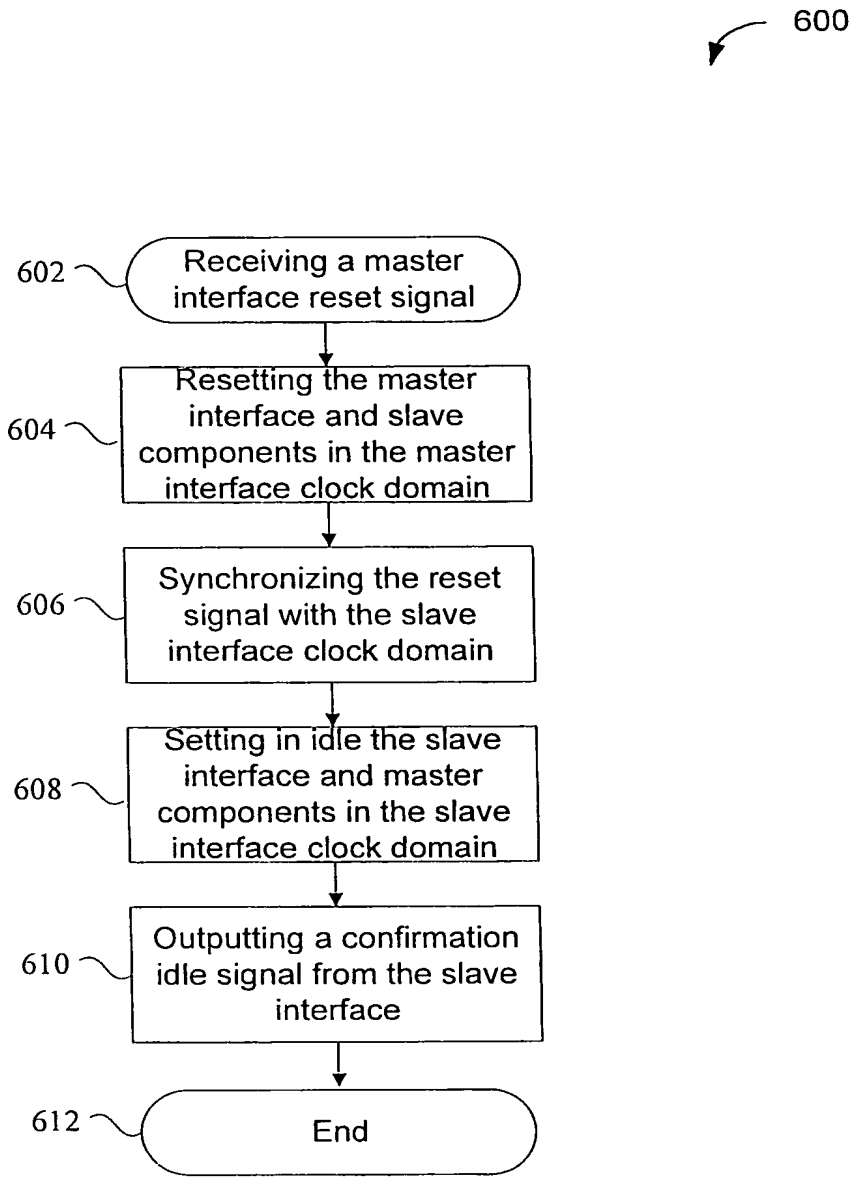
600
602
Receiving a master interface reset signal
604
Resetting the master interface and slave components in the master interface clock domain
606
Synchronizing the reset signal with the slave interface clock domain
608
Setting in idle the slave interface and master components in the slave interface clock domain
610
Outputting a confirmation idle signal from the slave interface
612
End

Figure 6

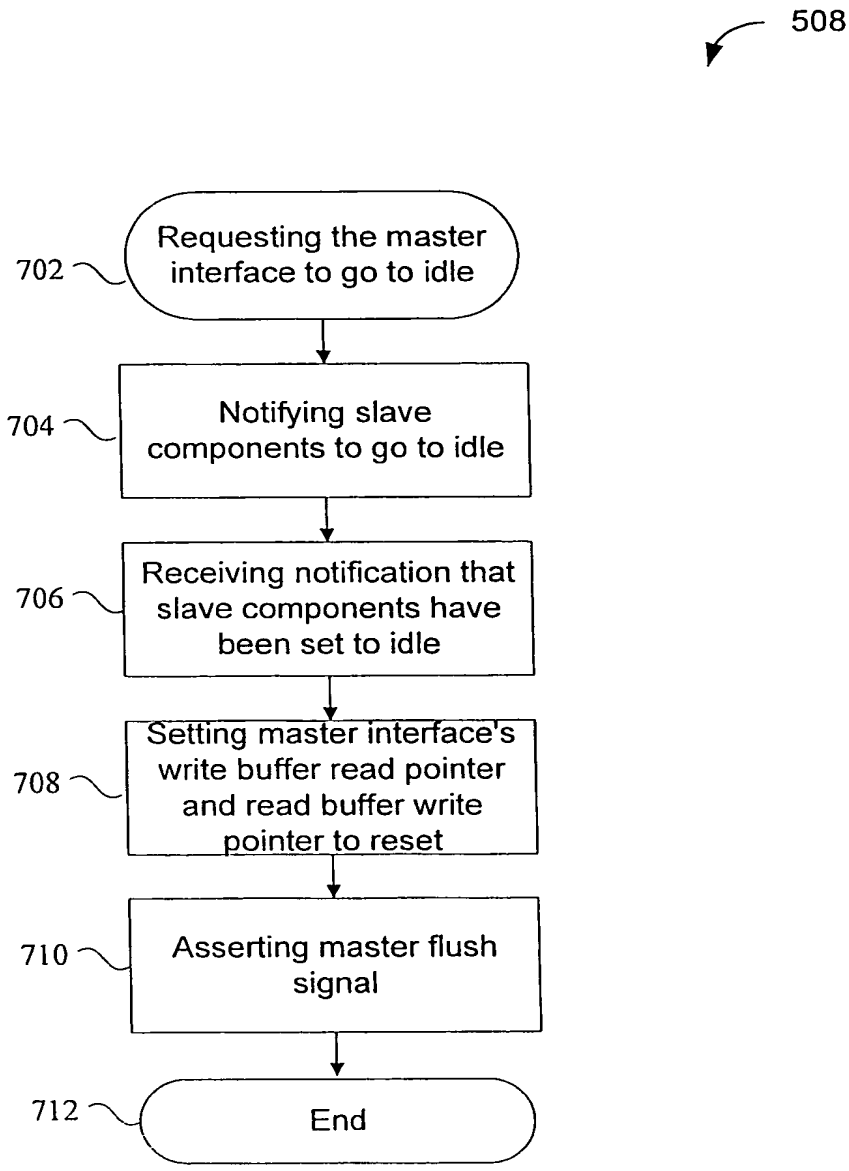
508
Requesting the master interface to go to idle
702
Notifying slave components to go to idle
704
Receiving notification that slave components have been set to idle
706
Setting master interface's write buffer read pointer and read buffer write pointer to reset
708
Asserting master flush signal
710
End
712

Figure 7

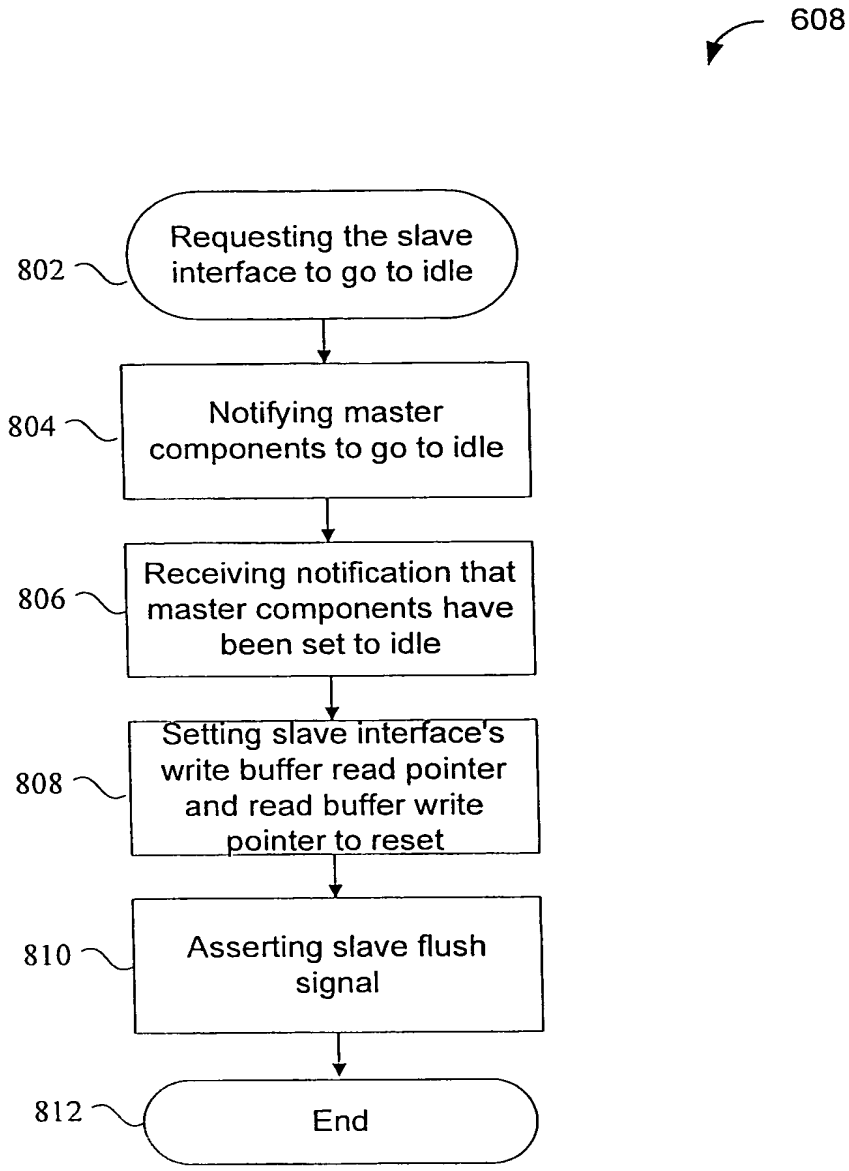
608
802
Requesting the slave interface to go to idle
804
Notifying master components to go to idle
806
Receiving notification that master components have been set to idle
808
Setting slave interface's write buffer read pointer and read buffer write pointer to reset
810
Asserting slave flush signal
812
End

Figure 8